

K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Nov – Dec 2025

(B. Tech) Program: Electronics and Telecommunication Scheme III

Regular Examination: SY Semester: III

Course Code: EXC302 and Course Name: Digital Logic Design

Max. Marks: 60

Date of Exam: **27/11/25**

Duration: 02.5 Hours

Instructions:

- (1) All questions are compulsory.
- (2) Draw neat diagrams wherever applicable.
- (3) Assume suitable data, if necessary.

Q. No.	Question	Max. Marks	CO	BT level
Q 1	Solve any two questions out of three: (05 marks each)	10		
a)	Convert i) $(123)_{10}$ in to binary ii) $(AB9)_{16}$ in to Decimal iii) $(351)_8$ in to decimal iv) 129 in to BCD		CO1	Ap
b)	Design 1 bit comparator circuit.		CO2	Ap
c)	Minimize the following expression using K-map technique $Y = \sum m(0,1,3,4,5)$		CO3	Ap
Q 2	Solve any two questions out of three: (05 marks each)	10		
a)	Design full adder circuit.		CO1	Ap
b)	Explain JK flip flop.		CO4	U
c)	Explain the features of VHDL.		CO6	U
Q.3	Solve any two questions out of three. (10 marks each)	20		
a)	i) Compare TTL and CMOS logic families with their characteristics. [5M] ii) Explain and Prove De Morgan's theorem [5M]		CO2	Ap
b)	Simplify equation using Quine McCluskey method and realize circuit using basic gates. $F(A,B,C,D) = \sum(1,4,5,6,7,9,13)$		CO3	U
c)	Explain 4-bit universal shift register in detail.		CO4	U
Q.4	Solve any two questions out of three. (10 marks each)	20		

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a)	i) Implement the following using only one 8:1 Mux. $F(A,B,C,D) = \pi M (0,3,5,6,8,9,10,12,14)$ [6M] ii) Design 2 to 8 line decoder with its circuit diagram [4M]	CO3	Ap
b)	Convert T Flip Flop into D Flip Flop.	CO4	Ap
c)	i) Compare SRAM and DRAM.[5M] ii) Compare PLA and PAL. [5M]	CO5	U
