**K. J. Somaiya Institute of Technology, Sion, Mumbai-22**
**(Autonomous College Affiliated to University of Mumbai)**

Nov – Dec 2025
(B. Tech)Program: EXTC Scheme I/II/IIB/III: III
Regular/Supplementary Examination: SY Semester: III
Course Code:EXC303 and Course Name: Electronic Devices and Linear circuits
Date of Exam: 02/12/2025 Duration: 02.5 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

| Q. No. | Question | Max. Marks | CO | BT level |
|---|---|---|---|---|
| Q 1 | Solve any **two** questions out of three: (05 marks each) | 10 | | |
| a) | Draw the basic circuit diagram of IC 566 as a VCO . | | 6 | U |
| b) | Explain N-Channel MOSFET characteristic. | | 1 | U |
| c) | Draw a neat block diagram off OP-AMP IC 741 also, compare its ideal and practical characteristic | | 2 | Ap |
| Q 2 | Solve any **two** questions out of three: (05 marks each) | 10 | | |
| a) | Design a 555 astable circuit to generate a 1 kHz signal with 60% duty cycle. | | 5 | U |
| b) | Explain Voltage to Current and Current to Voltage Converter. | | 3 | Ap |
| c) | Draw and Explain the circuit for Zero crossing Detector. | | 4 | U |
| Q.3 | Solve any **two** questions out of three. (10 marks each) | 20 | | |
| a) | Explain Phase locked loop using Block diagram. State role of all sub block of VCO used in PLL. | | 6 | Ap |
| b) | Draw summing amplifier circuit using opamp and Derive Vo for summing amplifier. | | 2 | An |
| c) | Explain half wave and Full wave precision rectifier. | | 4 | U |
| Q.4 | Solve any **two** questions out of three. (10 marks each) | 20 | | |
| a) | Explain the significance of biasing in a transistor amplifier. .Explain any One biasing circuits | | 1 | U |
| b) | Explain 555 IC Astable mode of operation. | | 5 | U |
| c) | Explain working of RC phase shift Oscillator. | | 3 | U |