K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
Supplementary Exam ~~Nov – Dec 2025~~ Jan. 2026.

B.Tech Program: **EXTC** Scheme: **III**
Regular Examination : **TY** Semester: **V**
Course Code : **EXC501** Course Name: **Digital VLSI Design**
Date of Exam: ~~24th Nov 25~~ 28/01/26 Duration: **2.5 Hours** Max. Marks:**60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		M	CO	BT
Q 1	Solve any **two** questions out of three: (05 marks each)	**10**		
a)	Draw the block diagram of 4-bit array multiplier		5	U
b)	Realize 2 input NAND gate using the pseudo-NMOS design style.		3	C
c)	Define: V_{OH}, V_{OL}, V_{IH}, V_{IL} and rise time.		2	R
Q 2	Solve any **two** questions out of three: (05 marks each)	**10**		
a)	Explain the charge-sharing problem in the Domino design style.		3	U
b)	Differentiate between NOR flash and NAND flash memory.		4	U
c)	Write any ten Lambda rules used in VLSI fabrication.		1	U
Q.3	Solve any **two** questions out of three. (10 marks each)	**20**		
a)	Realize 8:1 multiplexer using Transmission Gate.		3	C
b)	Derive the expression for V_{OH} and V_{IH} of a CMOS inverter.		2	U
c)	Design NOR based ROM to store the following data: 1101, 0011, 1010, 0110. Draw the stick diagram for the same.		4	C
Q.4	Solve any **two** questions out of three. (10 marks each)	**20**		
a)	Design a Soda Dispenser Machine upto FSM using the RTL design process.		6	C
b)	Derive the expressions of Carry bits of 4-bit Carry Look Ahead Adder. Realize the circuit using MODL.		5	An
c)	Explain the different types of parasitic capacitances in a MOSFET.		1	U

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Seat No.: