University of Mumbai

Examination 2020 under cluster __(Lead College: _____)

Examinations Commencing from 23rd December 2020 to 6th January 2021 and from 7th January 2021 to 20th January 2021

Program: Computer Engineering

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: **CSC304** and Course Name: **Digital Logic and Computer Architecture**

Time: 2 hour Max. Marks: 80

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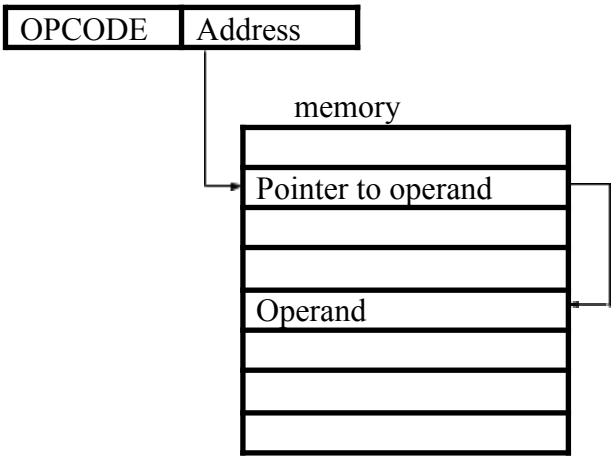
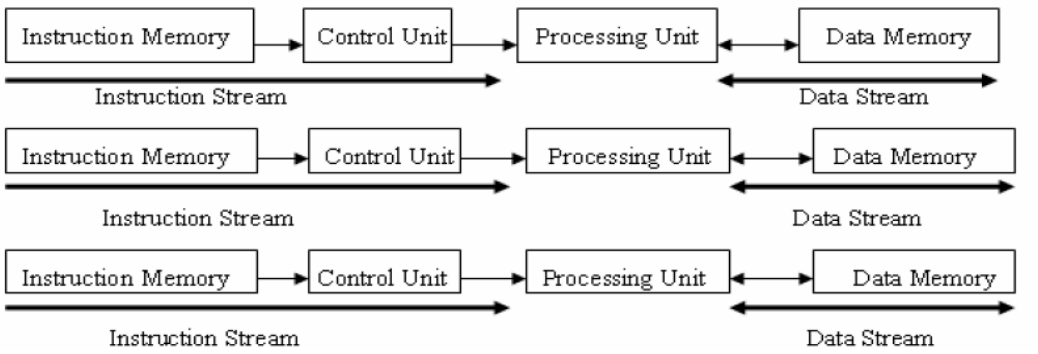
Q1. 40 Marks	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks (2 marks each)**
1.	Convert number(723.17)$_8$ into equivalent hexadecimal number
Option A:	(0D3.3C)16
Option B:	(1D3.3C)16
Option C:	(1E3.3C)16
Option D:	(1D3.4C)16
2.	What is the equivalent of $(52)_{10}$ in Gray code
Option A:	110100
Option B:	1011101
Option C:	111000
Option D:	101110
3.	As per Boolean Laws which of the expressions results in 0 (i) A+$\bar{A}$ (ii) A.$\bar{A}$ (iii)A.0 (iv) A. 1
Option A:	ii only
Option B:	ii &iii
Option C:	iii only
Option D:	ii,iii,iv
4.	For 4 bit number what is the range of 2's complement representation? Also perform $(5)_{10}$-$(7)_{10}$ using 2's complement method
Option A:	-7 to +7 , 1101
Option B:	-8 to +8 , 1110
Option C:	-8 to +7 , 1110
Option D:	-7 to +8 , 1101

5.	Arrange the steps for obtaining IEEE representation of floating point in proper format 1) calculate the biased exponent 2) convert to binary 3) convert to normalized form
Option A:	1,2,3
Option B:	3,2,1
Option C:	2,3,1
Option D:	2,1,3
6.	In Restoring division Algorithm if A<0 then which of the following is immediate step (Assume M as Dividend Q as Divisor and A as result)
Option A:	Q_0 =0
Option B:	A= A +M
Option C:	Q_0 =0 & A=A-M
Option D:	Q_0 =0 & A=A+M
7.	In full adder, Boolean expression of sum will be_____
Option A:	S=A XOR $\overline{B}$
Option B:	S=$\overline{A}$ XOR B
Option C:	S = A XOR B XOR C
Option D:	S = A XOR B XOR $\overline{C}$
8.	Which of the following Twos Complement binary numbers is equivalent to decimal −75 ?
Option A:	1001011
Option B:	1001100
Option C:	0001100
Option D:	0110101
9.	Identify the type of addressing mode Instruction 
Option A:	Register Addressing mode
Option B:	Register Indirect Addressing mode

Option C:	Direct Addressing mode
Option D:	Indirect Addressing mode
10.	Choose appropriate sequence of instruction cycle
Option A:	Instruction fetch, Instruction address calculation, Instruction decode, operand address calculation , fetch operand, data operation, operand address calculation, operand store
Option B:	Instruction address calculation , Instruction fetch, operand address calculation fetch operand, Instruction decode, data operation, operand address calculation and operand store
Option C:	Instruction address calculation , Instruction fetch, Instruction decode, operand address calculation , fetch operand, data operation , operand address calculation, operand store
Option D:	Instruction address calculation, Instruction fetch, Instruction decode, operand address calculation , fetch operand, operand address calculation , operand store, data operation
11.	Basic task for control unit is
Option A:	To perform logical operations
Option B:	Execution
Option C:	To initiate the resources
Option D:	To decode instructions and generate control signal
12.	A micro instruction has ____
Option A:	Control field
Option B:	Address field
Option C:	Status field
Option D:	Both control and address field
13.	Microprogram consisting of _____ is stored in control memory of control unit
Option A:	instructions
Option B:	micro instructions
Option C:	micro program
Option D:	macro program
14.	In memory Hierarchy which is the fastest memory
Option A:	SRAM
Option B:	DRAM
Option C:	Register
Option D:	Cache
15.	The correspondence between the main memory blocks and those in the cache is given by _____.
Option A:	Mapping function
Option B:	Hash function
Option C:	Locale function
Option D:	Assign function

16.	Consider a direct mapped cache of size 64 KB with block size 16 bytes. The CPU generates 28-bit addresses. The number of bits needed for cache indexing are respectively are:
Option A:	13
Option B:	10
Option C:	12
Option D:	11
17.	In Instruction Pipelining Structural Hazard means
Option A:	any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline
Option B:	a delay in the availability of an instruction causes the pipeline to stall
Option C:	the situation when two instructions require the use of a given hardware resource at the same time.
Option D:	When a data gets overwritten by branching
18.	Identify the Type of Flynn's Classification of Parallel Processing 
Option A:	SISD
Option B:	SIMD
Option C:	MISD
Option D:	MIMD
19.	To resolve the clash over the access of the System Bus we use
Option A:	BUS arbitrator
Option B:	Multiple BUS
Option C:	Priority access
Option D:	virtual access
20.	SIMD represents an organization that _____.
Option A:	refers to a computer system capable of processing several programs at the same time.
Option B:	represents organization of single computer containing a control unit, processor unit and a memory unit.
Option C:	includes many processing units under the supervision of a common control unit
Option D:	includes many processing units with many control unit.

Q2 **20 Marks**	**Solve any Four out of Six (5 marks each)**
A	Show the mathematical step for the following conversion i) Convert decimal (123.25) to its equivalent octal ii) Convert decimal (123.25) to its equivalent hexadecimal iii) Convert Hexadecimal (ABCD) to its equivalent binary iv) Convert binary (10111100) to equivalent gray code v) Convert decimal (1543) to Excess-3 code
B	Write short note on Von-Neumann Model
C	Explain the single and double precision format for representing floating point number using IEEE 754 standards
D	Define Instruction cycle. Explain it with a detailed state diagram.
E	Differentiate between static RAM and dynamic RAM.
F	What are the functions of following Register 1. IR 2. PC 3. MAR 4. MDR 5. SP

Q3. **20 marks**	
A	**Solve any Two Questions out of Three (5 marks each)**
i)	Write micro program for the instruction ADD A, B (Register A and B are added and result is stored at Register A.)
ii)	Differentiate between Hardwired control unit and Micro programmed control unit
iii)	Explain memory Hierarchy
B	**Solve any One Question out of two (10 marks each)**
i)	A program having 10 instructions (without Branch and Call instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsec. (Assume the four stages as Fetch Instruction ,Decode Instruction, Execute Instruction, Write Output) i. Calculate time required to execute the program on Non-pipeline and Pipeline processor. Ii Show the pipeline processor with a diagram.
ii)	Draw the flowchart of Restoring Division Algorithm & perform 10 /3 using this Algorithm

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	D
Q3.	B
Q4	C
Q5	C
Q6	D
Q7	C
Q8.	D
Q9.	D
Q10.	C
Q11.	D
Q12.	D
Q13.	B
Q14.	C
Q15.	A
Q16.	B
Q17.	C
Q18.	D
Q19.	A
Q20.	C

Note: The distribution of marks the for the descriptive questions is given below for your illustration. Examiners may vary with this and add additional criteria's for evaluation

Q2:

A. For every conversion allot 1 mark

B. Von-Neumann Model block diagram 2 marks and explanation 3 marks

C. For single precision allot 2,5 marks for describing format , specifying various fields and their size similarly for double precision 2.5 marks for describing format , specifying various fields and their size

D. Definition 1 mark , explanation of state diagram marks and for drawing state diagram 2 marks

E. For every main difference allot 1 mark

F. 1 mark each for every register function described

Q3.

A

i) . For defining the Micro program 4 marks and for explanation 1 mark

ii) For every main difference allot 1 mark

iii) For diagram allot 2 marks and for explanation 3 marks

B

i) for calculations of time required for Pipelined and non-Pipelined System allot 4 marks and for Drawing the timing diagram for Pipelined processor allot 6 marks

ii) For flow chart allot 4 marks and for performing the mathematical task of 10/3 allot 6 marks