University of Mumbai

Examination 2020 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examination Commencing from 7th January 2021 to 20th January 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III

Course Code: ELC303 and Course Name: Digital Logic Circuits

Time: 2 hour Max. Marks: 80

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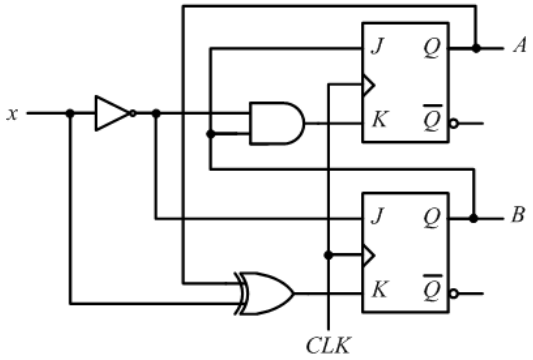
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	What is the decimal equivalent of $(11111)_2$.
Option A:	$(41)_{10}$
Option B:	$(21)_{10}$
Option C:	$(31)_{10}$
Option D:	$(11)_{10}$
2.	What is the reflected binary code of $(100101)_2$
Option A:	111000
Option B:	101010
Option C:	101111
Option D:	110111
3.	Given the two binary numbers x=1010100 and y=1000011 perform the subtraction x-y, using 2's complement.
Option A:	0010001
Option B:	1101110
Option C:	1111111
Option D:	0000111
4.	How many two-input AND and OR gates are required to realize Y = AB+CD+E?
Option A:	2,2
Option B:	2,3
Option C:	3,2
Option D:	3,3
5.	If a half adder has A and B as the inputs, then the sum is given by
Option A:	A EX-NOR B
Option B:	A OR B
Option C:	A AND B
Option D:	A XOR B
6.	What are the number of select lines required for a 8:1 multiplexer?
Option A:	1

Option B:	2
Option C:	3
Option D:	4
7.	A decoder converts ‘n’ inputs to _____ number of outputs.
Option A:	2^n
Option B:	n
Option C:	n^2
Option D:	2n
8.	A basic latch circuit consists of
Option A:	one comparator
Option B:	three adders
Option C:	two inverters
Option D:	one amplifier
9.	A ‘n-stage’ Johnson counter will circulate a single data bit giving sequence of ____ number of states.
Option A:	2n
Option B:	n
Option C:	n+1
Option D:	n^2
10.	A decade counter can be implemented with how many number of flip flops?
Option A:	10
Option B:	5
Option C:	4
Option D:	8
11.	MSI counter IC74163 is
Option A:	4 bit up counter with synchronous preset and clear
Option B:	ripple counter
Option C:	decade counter
Option D:	4 bit up counter with asynchronous preset and clear
12.	In a sequential circuit designed as a moore machine, the output depends on
Option A:	present state
Option B:	past state
Option C:	next state
Option D:	external inputs
13.	IC 7490 is a
Option A:	Group A Asynchronous counter IC
Option B:	Group B Asynchronous counter IC
Option C:	Group C Asynchronous counter IC
Option D:	synchronous counter
14.	The internal structure of MSI counter IC 7493 consist of

Option A:	Mod 2 and Mod 6 counter
Option B:	Mod 2 and Mod 8 counter
Option C:	Mod 5 and Mod 8 counter
Option D:	Mod 2 and Mod 5 counter
15.	An AND gate with 8 input has a fan-out of
Option A:	8
Option B:	4
Option C:	2
Option D:	1
16.	What does FPGA stand for
Option A:	Field Programming Gate Array
Option B:	Field Programmable Gate Array
Option C:	First Program Gate Array
Option D:	First Programmable Gate Array
17.	Programmable Array Logic has
Option A:	a programmable AND and fixed OR array
Option B:	a programmable AND and a programmable OR array
Option C:	only a programmable AND array
Option D:	only a programmable OR array
18.	In verilog HDL the operator <= is used for
Option A:	Blocking assignment
Option B:	Non-Blocking assignment
Option C:	Single line comment
Option D:	Logical left shift
19.	Which type of modeling style is not used in verilog hardware description language
Option A:	Structural
Option B:	Datatype
Option C:	Behavioral
Option D:	Data Flow
20.	The Verilog expression for Boolean equation Y=AB+C will be
Option A:	assign Y= (A*B)+C
Option B:	assign Y= (A.B)+C
Option C:	assign Y= (A^B)|C
Option D:	assign Y= (A&B)|C

Q2. **(20 Marks Each)**	
A	**Solve any Two 5 marks each**
i.	Design and implement a half adder using gates.
ii.	State and prove De-Morgan's theorem.
iii.	Compare mealy and moore machines.
B	**Solve any One 10 marks each**
i.	Design a Mod-10 asynchronous counter using J-K Flip–Flops.
ii.	Write a program using Verilog HDL to implement a 8:1 multiplexer.

Q3. **(20 Marks Each)**	
A	**Solve any Two 5 marks each**
i.	Write a short note on Complex Programmable Logic Devices.
ii.	Convert a JK Flip-Flop to T Flip-Flop.
iii.	Write a program for a D flip-flop with asynchronous reset using Verilog HDL.
B	**Solve any One 10 marks each**
i.	Design and implement full subtractor circuit using a 3:8 decoder IC 74138.
ii.	Analyze the given state machine and draw the state diagram. 

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Q1:

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	D
Q3.	A
Q4	A
Q5	D
Q6	C
Q7	A
Q8.	C
Q9.	A
Q10.	C
Q11.	A
Q12.	A
Q13.	A
Q14.	B
Q15.	D
Q16.	B
Q17.	A
Q18.	B
Q19.	B
Q20.	D

Important steps and final answer for the questions involving numerical example

Q2(A) i: Step 1:Truth Table of Half Adder

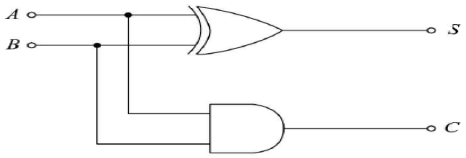
Inputs		Outputs	
A	*B*	*S*	*C*
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Step 2:

$S = \overline{A}B + A\overline{B} = A \oplus B$

C= A.B

Step 3:



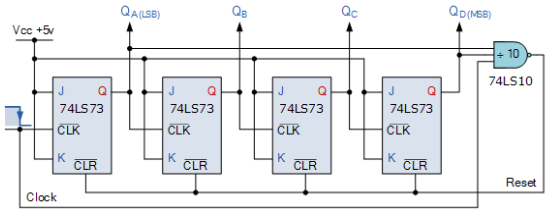
Q2 (B) i

Step 1:Truth table of Mod 10 counter

Clock Count	Output bit Pattern				Decimal Value
	QD	QC	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

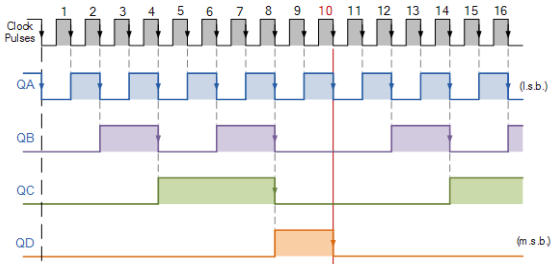
Step 2:

Circuit Diagram



Step 3:

Timming Diagram



Q2 (B)(ii)

```
module Mulitplexer(d0,d1,d2,d3,d4,d5,d6,d7,sel,out);
    input d0,d1,d2,d3,d4,d5,d6,d7;
    input [2:0] sel;
    output reg out;
    always@(sel)
    begin
        case(sel)
            3'b000:out=d0;
            3'b001:out=d1;
            3'b010:out=d2;
            3'b011:out=d3;
            3'b100:out=d4;
            3'b101:out=d5;
            3'b110:out=d6;
            3'b111:out=d7;
        endcase
    end
endmodule
```

Q3 A(ii)

Truth Table of D Flip-flop

Input	Outputs	
	Present State	Next State
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

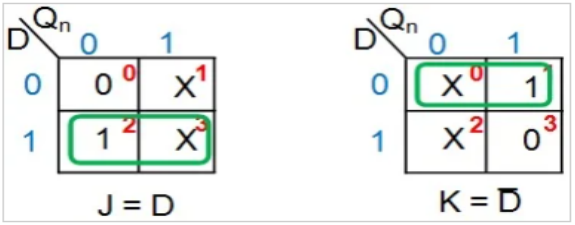
Excitation Table of JK Flip-flop

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

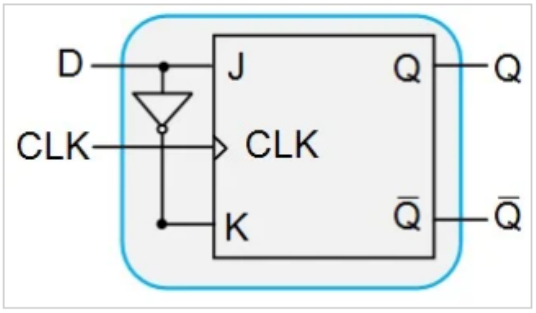
J-K to D conversion Table

D Input	Outputs		JK Inputs	
	Present State	Next State		
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

K-Map



Circuit Diagram:



Q3A(iii)

```
module DFlipFlop (D, clk, reset, Q);
input D; // Data input
input clk; // clock input
input reset; // asynchronous reset
output reg Q; // output Q
always @(posedge clk or posedge reset)
begin
 if(reset==1'b1)
  Q <= 1'b0;
 else
  Q <= D;
end
endmodule
```

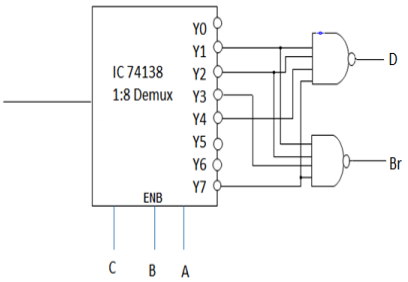
Q3 B(i) Truth Table of Full Subtractor

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$D = \sum m(1, 2, 4, 7)$

$B = \sum m(1, 2, 3, 7)$

Circuit Diagram:



Q3 B(ii)

Flip –Flop Equations:

$J_A = B$ $K_A = B\ x'$

$J_B = x'$ $K_B = A \oplus x$

Next State Equations:

$A(t+1) = J_A Q'_A + K'_A Q_A$

$= A'B + AB' + Ax$

$B(t+1) = J_B Q'_B + K'_B Q_B$

$= B'x' + ABx + A'Bx'$

State Table:

Present State		I/P	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Transition Diagram