University of Mumbai

Examination 2020 under cluster 5 (Lead College: APSIT)

Examinations Commencing from 23rd December 2020 to 6th January 2021 and from 7th January 2021 to 20th January 2021

Program: **Electronics and Telecommunication**

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ECC303 and Course Name: Digital System Design

Time: 2 Hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	A full adder can be made out of ……
Option A:	two half adders
Option B:	two half adders and a OR gate
Option C:	two half adders and a NOT gate
Option D:	three half adders
2.	POS expressions can be implemented using ……logic circuit.
Option A:	2-level OR-AND
Option B:	2-level OR-AND and NOR
Option C:	2-level XOR
Option D:	2-level NOR
3.	To program basic logic functions which type of PLD should be used?
Option A:	PAL
Option B:	PLA
Option C:	CPLD
Option D:	SLD
4.	Sequential structure of VHDL
Option A:	Library Declaration; Configuration; Entity Declaration; Architecture Declaration
Option B:	Library Declaration; Entity Declaration; Configuration; Architecture Declaration
Option C:	Library Declaration; Configuration; Architecture Declaration; Entity Declaration
Option D:	Library Declaration; Entity Declaration; Architecture Declaration; Configuration
5.	VHDL is based on which programming language
Option A:	C
Option B:	PHP
Option C:	Assembly
Option D:	ADA
6.	TTL inputs are the emitters of a _____
Option A:	Transistor-transistor logic
Option B:	Multiple-emitter transistor
Option C:	Resistor-transistor logic
Option D:	Diode-transistor logic

7.	In case of XOR/XNOR simplification we have to look for the following_____
Option A:	Both Diagonal and Straight Adjacencies
Option B:	Only Offset Adjacencies
Option C:	Both Offset and Straight Adjacencies
Option D:	Both Diagonal and Offset Adjacencies
8.	On addition of 28 and 18 using 2's complement, we get
Option A:	00101110
Option B:	0101110
Option C:	00101111
Option D:	1001111
9.	One example of the use of an S-R flip-flop is as
Option A:	Transition pulse generator
Option B:	Racer
Option C:	Switch debouncer
Option D:	Astable oscillator
10.	Being a universal gate, it is possible for NOR gate to get converted into AND gate by inverting the inputs _____.
Option A:	before getting applied to NOR gate
Option B:	after getting applied to NOR gate
Option C:	before getting applied to AND gate
Option D:	after getting applied to AND gate
11.	On subtracting (01010)2 from (11110)2 using 1's complement, we get _____
Option A:	01001
Option B:	11010
Option C:	10101
Option D:	10100
12.	Which of the following is the most widely employed logic family?
Option A:	Emitter-coupled logic
Option B:	Transistor-transistor logic
Option C:	CMOS logic family
Option D:	NMOS logic
13.	The time required for a gate or inverter to change its state is called
Option A:	Rise time
Option B:	Decay time
Option C:	Propagation time
Option D:	Charging time
14.	Internal propagation delay of asynchronous counter is removed by _____
Option A:	Ripple counter
Option B:	Ring counter
Option C:	Modulus counter

Option D:	Synchronous counter
15.	One of the major drawbacks to the use of asynchronous counters is that
Option A:	Low-frequency applications are limited because of internal propagation delays
Option B:	High-frequency applications are limited because of internal propagation delays
Option C:	Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
Option D:	Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications
16.	What is the preset condition for a ring shift counter?
Option A:	All FFs set to 1
Option B:	All FFs cleared to 0
Option C:	A single 0, the rest 1
Option D:	A single 1, the rest 0
17.	In a positive edge triggered JK flip flop, a low J and low K produces?
Option A:	High state
Option B:	Low state
Option C:	Toggle state
Option D:	No Change State
18.	Which is the major functioning responsibility of the multiplexing combinational circuit?
Option A:	Decoding the binary information
Option B:	Generation of all minterms in an output function with OR-gate
Option C:	Generation of selected path between multiple sources and a single destination
Option D:	Encoding of binary information
19.	The octal number (651.124)8 is equivalent to _____
Option A:	(1A9.2A)16
Option B:	(1B0.10)16
Option C:	(1A8.A3)16
Option D:	(1B0.B0)16
20.	The addition of +19 and +43 results as in 2's complement system.
Option A:	11001010
Option B:	101011010
Option C:	00101010
Option D:	0111110

Subjective/Descriptive Questions

Option 1

Q2 **(Total 20 Marks)**	**Solve any Four out of Six** **5 marks each**
A	Compare SRAM with DRAM.
B	Design full adder using 3:8 decoder.
C	Convert (532.125) base 8, into decimal, binary and hexadecimal.
D	VHDL Code for full Adder.
E	Convert JK Flip Flop to T Flip Flop.
F	Compare TTL and CMOS Logic Families.

Option 2

Q3. **(Total 20 Marks)**	**Solve any Two Questions out of Three** **10 marks each**
A	Design 3 bit gray to binary converter.
B	Minimize the following expression using Quine Mc-cluskey technique. $F(A,B,C,D)=\sum M(0,1,2,3,5,7,9,11)$
C	Design Synchronous counter using T-type flip flops for getting the following sequence 0-2-4-6-0.take care of lockout condition.

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	B
Q3.	A
Q4	D
Q5	D
Q6	B
Q7	D
Q8.	B
Q9.	C
Q10.	A
Q11.	D
Q12.	B
Q13.	C
Q14.	D
Q15.	B
Q16.	D
Q17.	D
Q18.	C
Q19.	A
Q20.	D